This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims

1. (Currently amended) A semiconductor structure comprising:

a first semiconductor layer having a plurality of threading dislocations distributed substantially uniformly across a surface thereof, defining a threading dislocation density of the first semiconductor layer that varies across the surface by no more than one order of magnitude; and

a relaxed compositionally uniform cap layer disposed over the surface of the first semiconductor layer~~, the cap layer being substantially relaxed~~.

2. (Currently amended) The semiconductor structure of claim 1 wherein a lattice constant of the compositionally uniform cap layer is different from a lattice constant of the first semiconductor layer.

3. (Original) The semiconductor structure of claim 1 further comprising:

a strained semiconductor layer disposed over the compositionally uniform cap layer.

4. (Original) The semiconductor structure of claim 3 wherein the strained semiconductor layer is tensilely strained.

5. (Original) The semiconductor structure of claim 4 wherein the strained semiconductor layer comprises tensilely strained silicon or tensilely strained silicon-germanium alloy.

6. (Original) The semiconductor structure of claim 3 wherein the strained semiconductor layer is compressively strained.

7. (Original) The semiconductor structure of claim 6, wherein the strained semiconductor layer comprises compressively strained germanium or compressively strained silicon-germanium alloy.

8. (Original) The semiconductor structure of claim 1 wherein the compositionally uniform cap layer comprises at least one of a group II, a group III, a group IV, a group V, and a group VI element.

9. (Original) The semiconductor structure of claim 8 wherein the compositionally uniform cap layer comprises at least one of silicon and germanium.

10. (Original) The semiconductor structure of claim 9 wherein the compositionally uniform cap layer comprises more than approximately 10% germanium.

11. (Currently amended) The semiconductor structure of claim 1 wherein [[the]]a thickness of the compositionally uniform cap layer is selected from a range[[s]] of~~from~~ about 0.5 μm to about 3.0 μm.

12. (Currently amended) The semiconductor structure of claim 1 wherein the compositionally uniform cap layer is planarized.

13. (Withdrawn) The semiconductor structure of claim 1 further comprising:

a compositionally graded layer disposed between the compositionally uniform cap layer and the first layer.

14. (Withdrawn) The semiconductor structure of claim 13 wherein the graded layer comprises at least one of a group II, a group III, a group IV, a group V, and a group VI element

15. (Withdrawn) The semiconductor structure of claim 14 wherein the graded layer comprises at least one of silicon and germanium.

16. (Withdrawn) The semiconductor structure of claim 15 wherein the graded layer has a grade rate greater than about 5% germanium per micrometer.

17. (Withdrawn) The semiconductor structure of claim 16 wherein the graded layer has a grade rate less than about 50% germanium per micrometer.

18. (Withdrawn) The semiconductor structure of claim 13 wherein the graded layer is graded to a concentration of greater than about 10% germanium.

19. (Withdrawn) The semiconductor structure of claim 13 wherein the thickness of the graded layer ranges from about 0.5 μm to about 10.0 μm.

20. (Withdrawn) The semiconductor structure of claim 13 wherein the first layer comprises an initial portion of the graded layer; the initial portion having a lower local grading rate than at least one subsequent portion of the graded layer and wherein the threading dislocations are uniformly distributed in the initial portion.

21. (Withdrawn) The semiconductor structure of claim 20 wherein the graded layer comprises at least one of silicon and germanium.

22. (Withdrawn) The semiconductor structure of claim 21 wherein the difference in local grading rate is greater than about 5% Ge/μm.

23. (Withdrawn) The semiconductor structure of claim 22 wherein the difference in local grading rate is greater than about 20% Ge/μm.

24. (Withdrawn) The semiconductor structure of claim 21 wherein the grading rate of the initial portion of the relaxed graded buffer layer does not exceed about 10% Ge/μm.

25. (Withdrawn) The semiconductor structure of claim 21 wherein the discontinuity in Ge content at the interface between the initial portion and at least one subsequent portion of the relaxed graded layer does not exceed about 10% Ge.

26. (Withdrawn) The semiconductor structure of claim 25 wherein the discontinuity in Ge content at the interface between the initial portion and at least one subsequent portion of the relaxed graded buffer layer does not exceed about 5% Ge.

27. (Withdrawn) The semiconductor structure of claim 1 wherein the first layer comprises a seed layer disposed proximal to the surface of the first layer and wherein the threading dislocations are uniformly distributed in the seed layer.

28. (Withdrawn) The semiconductor structure of claim 27 wherein the seed layer is at least partially relaxed.

29. (Withdrawn) The semiconductor structure of claim 27 wherein the seed layer is compositionally uniform.

30. (Withdrawn) The semiconductor structure of claim 27 wherein the seed layer is compositionally graded.

31. (Withdrawn) The semiconductor structure of claim 27 wherein the thickness of the seed layer is greater than twice its equilibrium critical thickness.

32. (Withdrawn) The semiconductor structure 31 wherein the thickness of the seed layer is less than about five times its equilibrium critical thickness.

33. (Withdrawn) The semiconductor structure 27 wherein at least a portion of the seed layer is formed by growth at a growth temperature of about 850°C.

34. (Withdrawn) The semiconductor structure 27 wherein at least a portion of the seed layer is formed by growth at a growth temperature above 1000 °C.

35. (Withdrawn) The semiconductor structure 27 wherein the seed layer has a thickness ranging from about 10 nm to about 1000 nm.

36. (Withdrawn) The semiconductor structure 35 wherein the seed layer has a thickness ranging from about 30 nm to about 300 nm.

37. (Withdrawn) The semiconductor structure 27 wherein the cap layer has a density of dislocation pile-ups of less than about 1/cm.

38. (Withdrawn) The semiconductor structure 27 wherein the cap layer has a density of dislocation pile-ups of less than 0.01/cm.

39. (Withdrawn) The semiconductor structure 27 wherein the cap layer has a threading dislocation density of less than about $5 \times 10^5/cm^2$.

40. (Withdrawn) The semiconductor structure of claim 27, further comprising:

a compositionally uniform buffer layer disposed between the compositionally uniform cap layer and the seed layer.

41. (Withdrawn) The semiconductor structure of claim 40 wherein the buffer layer comprises silicon.

42. (Withdrawn) The semiconductor structure of claim 40 wherein at least one of the buffer layer and the seed layer comprises at least one of silicon and germanium.

43. (Withdrawn) The semiconductor structure of claim 42 wherein a concentration of germanium in the buffer layer is different than a concentration of germanium in the seed layer at an interface between the seed layer with the buffer layer.

44. (Withdrawn) The semiconductor structure of claim 43 wherein discontinuity in germanium concentration at an interface between the seed layer with the buffer layer ranges from about 2% to 50% Ge.

45. (Withdrawn) The semiconductor structure of claim 44 wherein discontinuity in germanium concentration at an interface between the seed layer with the buffer layer ranges from about 5% to 15% Ge.

46. (Withdrawn) The semiconductor structure of claim 45 wherein discontinuity in germanium concentration at an interface between the seed layer with the buffer layer comprises about 10% Ge.

47. (Withdrawn) The semiconductor structure of claim 27, further comprising a compositionally graded layer disposed between the compositionally uniform cap layer and the seed layer.

48. (Withdrawn) The semiconductor structure of claim 47 wherein at least one of the graded layer and the seed layer comprises at least one of silicon and germanium.

49. (Withdrawn) The semiconductor structure of claim 47 wherein a concentration of germanium in the graded layer is different from a concentration of germanium in the seed layer at an interface between the seed layer with the graded layer.

50. (Withdrawn) The semiconductor structure of claim 49 wherein discontinuity in germanium concentration at an interface between the seed layer with the graded layer ranges from about 2% to 50% Ge.

51. (Withdrawn) The semiconductor structure of claim 50 wherein discontinuity in germanium concentration at an interface between the seed layer with the graded layer ranges from about 5% to 15% Ge.

52. (Withdrawn) The semiconductor structure of claim 51 wherein discontinuity in germanium concentration at an interface between the seed layer with the graded layer comprises about 10% Ge.

53. (Withdrawn) The semiconductor structure of claim 47, further comprising at least one intermediate seed layer disposed within the graded layer.

54. (Currently amended) The semiconductor structure of claim 1 wherein the first semiconductor layer comprises a silicon-on-insulator substrate.

55. – 77. (Cancelled)

78. (Original) The semiconductor structure of claim 1 wherein the compositionally uniform cap layer has an average surface roughness less than about 1 nm.

79. – 80. (Cancelled)

81. (New) The semiconductor structure of claim 1 wherein the relaxed compositionally uniform cap layer has a density of dislocation pile-ups of less than about 1/cm.

82. (New) The semiconductor structure of claim 1 wherein the relaxed compositionally uniform cap layer has a density of dislocation pile-ups of less than 0.01/cm.

83. (New) The semiconductor structure of claim 1 wherein the relaxed compositionally uniform cap layer has a threading dislocation density of less than about $5 \times 10^5/cm^2$.